

REMARKS

Claims 1-6 and 11-28 are pending. Claims 19 and 20 have been amended with this response to include the (believed) allowable elements of allowed independent claims 1, 23 and 28. Reconsideration of the application is respectfully requested based on the following remarks.

I. ALLOWED SUBJECT MATTER

Applicant acknowledges with appreciation the allowance of claims 1-6, 11-18 and 23-28.

II. REJECTION OF CLAIMS 19-22 UNDER 35 U.S.C. § 103(a)

Claims 19-22 were rejected under 35 U.S.C. § 103(a), as being unpatentable over U.S. Patent No. 7142671 to Qi et al. (hereinafter Qi) in view of US Patent 5099517 to Gupta (hereinafter Gupta). Withdrawal of the rejection is respectfully requested for at least the following reasons.

- i. **Neither Qi nor Gupta teach or suggest a security processing circuit comprising a clock input coupled to the single DES engine for timing clock cycles of the first, second and third single DES processing operations, as recited in claim 19.***

Independent claim 19 has been amended to include the (believed) allowable element of claims 1, 23 and 28 (**a clock input coupled to the single DES engine for timing clock cycles of the first, second and third single DES processing operations**), with the exception of the final alternate (or'd) elements: **a.** "wherein the 3DES processing is completed in eight clock cycles (claims 1 and 28), or **b.** wherein the first, second and third DES processing operations have a duration comprising two clock cycles each (claims 1 and 23)". Neither Qi nor Gupta teach or suggest this **clock input to the single DES engine and timing clock cycles of the first, second and third single**

DES processing operations. Thus claim 19 is not believed to be anticipated by Qi or Qi in view of Gupta, for at least this additional reason.

Accordingly, not all features of independent claim 19 are disclosed by Qi, or Qi in view of Gupta, and withdrawal of the rejection of claim 19 and claims 20-22 which depend therefrom is respectfully requested.

- ii. ***Neither Qi nor Gupta teach or suggest a security processing circuit comprising a clock input coupled to the single DES engine for timing clock cycles of the first, second and third single DES processing operations,***
 - a. ***wherein the 3DES processing is completed in eight clock cycles,***
or
 - b. ***wherein the first, second and third DES processing operations have a duration comprising two clock cycles each, as recited in claim 20.***

In addition, independent claim 20 has been amended to include the allowable elements of claims 1, 23 and 28, including the final alternate (or'd) elements: **a.** “*wherein the 3DES processing is completed in eight clock cycles (claims 1 and 28), or* **b.** *wherein the first, second and third DES processing operations have a duration comprising two clock cycles each (claims 1 and 23)”*. Neither Qi nor Gupta teach or suggest this **clock input to the single DES engine and wherein the 3DES processing is completed in eight clock cycles, or wherein the first, second and third DES processing operations have a duration comprising two clock cycles each**. Thus claim 20 is not believed to be anticipated by Qi or Qi in view of Gupta, for at least this additional reason.

Accordingly, not all features of claim 20 are disclosed by Qi or Qi in view of Gupta, and favorable acceptance of the claim is respectfully requested.

III. CONCLUSION

For at least the above reasons, the claims currently under consideration are believed to be in condition for allowance.

Should the Examiner feel that a telephone interview would be helpful to facilitate favorable prosecution of the above-identified application, the Examiner is invited to contact the undersigned at the telephone number provided below.

Should any fees be due as a result of the filing of this response, the Commissioner is hereby authorized to charge the Deposit Account Number 50-1733, AMDP783US.

Respectfully submitted,
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